REMARKS

The Examiner rejected claims 1 to 8 under 35 USC 102(b) as being anticipated by Poulo et al (US Patent Number 5,111,133). Applicant respectfully traverses this rejection.

Claim 1 requires "a comparator configured to compare a first signal with a second signal, said first signal having a DC offset determined, at least in part, by a DC reference voltage source, said second signal representative of an output voltage level of said DC to DC converter." For example, FIG. 8 of Applicant's specification illustrates a comparator 118 comparing a first signal received at its noninverting input terminal having a DC offset determined, at least in part, by the DC reference source 114 with a second signal received at its inverting input terminal.

In contrast to that required by claim 1, Poulo teaches a comparator 32 of Poulo's FIG. 8 that compares inductor current at its noninverting input terminal (column 5, lines 49 – 52) with the output of the junction 56 at its inverting input terminal. Poulo teaches that "it is the preferred approach to generate a compensating signal which is added to the desired current signal Id so that the analog input to the comparator 32 adapts to changes in the supply and voltages loads V^+, V^-, and V_L) in addition to those changes in the input voltage (or current)." Column 6, lines 6 – 10. Poulo goes on to teach that the compensating signal is preferably provided as a ramp signal from ramp generator 58 and "an additional correction signal Ic is generated and added to the ramp signal." Column 6, line 18 – 19.

This correction signal Ic provided by the multiplier/divider 54 is based on output signals from the "adders and subtractors circuit 52". Column 9, lines 7 – 13. The inputs to the adders and subtractors circuit 52 are V^+, V^-, and V_L, where V^+ and V^- are the positive and negative rail supply voltages (column 5, lines 26 – 29) and V_L is the load voltage across the inductor 26. See

also FIG. 8 of Poulo and column 6, lines 9 – 10. Therefore, importantly, the ramp signal provided by the ramp generator 58 of Poulo does not have "a DC offset determined, at least in part, by a DC reference voltage source" as required by claim 1. In fact, there is no reference voltage source taught, disclosed, or suggested by Poulo that could provide such a DC offset.

In addition, claim 1 requires "an accuracy circuit configured to provide a predetermined offset voltage value to one of said first signal and said second signal based on a difference between a DC voltage level of said DC reference voltage source and said output voltage of said DC to DC converter." For example, the accuracy circuits 802, 902 of Applicant's FIGs. 8 and 9 receive a signal along respective paths 810, 910 representative of the output voltage of the DC to DC converter and receive signals along respective paths 812, 912 representative of the DC voltage level of the DC reference source 114 in the embodiments of FIGs. 8 and 9. The accuracy circuits 802, 902 then provide on offset voltage value based on a difference between the DC voltage level of the DC reference source 114 and the output voltage of the DC to DC converter.

In contrast, the compensating signal generator 50 of Poulo provides a compensating signal to the desired Id current signal based on the output of the ramp generator 58 and multiplier/divider 54 which in turn is based on the values of V^+, V^-, and V_L. In other words, the compensating signal provide by the compensating signal generator 50 of Poulo is not based on a difference between a DC voltage level of a DC reference voltage source and an output voltage of the DC to DC converter as required by claim 1.

Accordingly, Applicant respectfully requests that the rejection of claim 1 under 35 USC 102(b) be withdrawn upon reconsideration. Claims 2 to 8 depend directly or indirectly from claim 1 and, as such, incorporate the limitations of claim 1. Accordingly, Applicant respectfully

submits that claims 2 to 8 are in condition for allowance for the reasons above adduced relative to claim 1 as well as for their own limitations.

The Examiner also rejected claims 9 - 10 under 35 USC 102(b) as being anticipated by Wilcox et al (US Patent No. 5,847,554). Applicant respectfully traverses this rejection. Wilcox teaches sensing circuitry 320 in FIG. 3 that "senses the voltage drops across both the regulator's main and synchronous switching elements as each in turn conducts (i.e., are ON). The sensed voltage drops are then combined and converted into an analog waveform indicative of the inductor current." Column 4, lines 57 – 62. Therefore, such regulators "do not require a current sensing element," (column 4, lines 52 – 53) and "[t]he elimination of the current sensing element results advantageously in reduced dissipative losses and manufacturing complexity." Column 4, lines 54 – 56.

The comparator 120 of Wilcox's FIG. 3 is similar to the comparator of Wilcox's FIG. 1 as Wilcox indicates "[w]hile regulator 300 is similar to regulator 100 of FIG. 1, differences include the absence of a current sensing element (e.g., current sense resistor 102) and the manner in which inductor current is sensed." Column 5, lines 27 – 30. With reference to FIG. 1, Wilcox explains the comparator 120 compares a differential sense voltage V_{SENSE} with a voltage across the threshold-setting resistor 118 and rests latch 106 when V_{SENSE} exceeds such voltage. Column 1, lines 57 – 65. Thus it can be seen that comparator 120 is not "a comparator configured to compare a first signal with a second signal, said first signal <u>having a DC offset determined, at least in part, by a DC reference voltage source</u>, said second signal representative of an output voltage level of said DC to DC converter" as required by claim 9.

FIG. 9 of Wilcox illustrates "a voltage-mode synchronous switching regulator 900." Column 7, lines 1 – 2. The comparator 954 of FIG. 9 is part of the sensing circuitry 920. With reference to a voltage-mode embodiment, Wilcox explains the "sensing circuitry senses the voltage drop across the synchronous switching elements as it conducts. When the sensed voltage exceeds a predetermined threshold, control circuitry reduces the regulator's duty cycle (i.e., keeps the main switching element OFF) to limit current while the output voltage is out of regulation." Column 5, lines 1 – 7.

Wilcox further explains that the "operation of the comparator 954 … is similar to that of comparator 222 (of FIG. 2) …" Column 7, lines 43 – 47. With reference to FIG. 2, Wilcox explains that "[d]uring normal operation only one parameter, output voltage V_{OUT}, is used to set the regulator's duty cycle. This is accomplished by pulse-width-modulator 212, which varies the pulse width of output signal 214 in response to V_{OUT}." Column 2, line 67 to Column 3, line 4. Wilcox further explains the purpose of comparator 222 is its use as part of a fault loop that includes the comparator 222, AND gate 220, and threshold voltage 224. "Thus if the drain-to-source voltage of MOSFET 202 exceeds threshold voltage 224 while MOSFET 202 is ON, a fault signal is sent to pulse-width-modulator 212 that responds by reducing ON-portion 215 of signal 214 to limit the amount of current to non-destructive levels." Column 3, lines 12 – 17. Therefore, the comparator 954 of Wilcox's FIG. 9 does not receive a signal "having a DC offset determined, at least in part, by a DC reference voltage source" as required by claim 9.

Accordingly, Applicant respectfully requests that the rejection of claim 9 under 35 USC 102(b) be withdrawn upon reconsideration. Claim 10 depends directly from claim 9 and, as such, incorporate the limitations of claim 9. Accordingly, Applicant respectfully submits that

claim 10 is in condition for allowance for the reasons above adduced relative to claim 9 as well as for its own limitations.

The Examiner also rejected claims 11 – 16 under 35 USC 103 as being unpatentable over Poulo et al (US Patent No. 5,111,133) in combination with Nerone (US Patent No. 5,859,504). Applicant respectfully traverses this rejection. As earlier detailed with respect to claims 1 to 8, Poulo does not teach, disclose, or suggest "a comparator configured to compare a first signal with a second signal, said first signal having a DC offset determined, at least in part, by a DC reference voltage source, said second signal representative of an output voltage level of said DC to DC converter." Nerone does not supply this missing teaching. Nerone is concerned with a ballast for a gas discharge lamp. Column 1, lines 19 – 24.

In light of the foregoing remarks, it is believed that all of the presently pending claims are in a condition for allowance. Allowance of the application is respectfully requested. In the event the Examiner deems personal contact desirable in disposition of this application, the Examiner is respectfully requested to call the undersigned attorney at (603) 668-6560.

In the event there are any fee deficiencies, please charge them (or credit any overpayment) to our Deposit Account No. 50-2121.

Respectfully submitted,

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